

Krenz *Instrumentation*

M2i.70xx - 64 bit fast digital I/O with TTL levels

- 16, 32 or 64 bit digital I/O
- 1 kS/s up to 125 MS/s at 16 and 32 bit
- 1 kS/s up to 60 MS/s at 32 and 64 bit
- 110 Ohm input impedance selectable
- Inputs 3.3 V and 5 V TTL compatible, Outputs 3.3 V
- Up to 4 GByte on-board memory
- 64 MByte standard memory installed
- FIFO mode for input and output
- Pattern/edge/pulse width/delay trigger
- Synchronization of up to 16 cards per system and up to 271 cards with system sync
- Options: Multiple Recording/Replay, Gated Sampling/Replay, BaseXIO



- 66 MHz 32 Bit PCI-X interface
- 5V / 3.3V PCI compatible
- 100% compatible to conventional PCI > V2.1
- Sustained streaming mode up to 225 MB/s

- 2,5 GBit x1 PCIe Interface
- Works with x1/x4/x8/x16* PCIe slots
- Software compatible to PCI
- Sustained streaming mode up to 160 MB/s

<u>Operating Systems</u>	<u>Recommended Software</u>	<u>Drivers</u>
<ul style="list-style-type: none"> • Windows 2k, XP, Vista • Linux Kernel 2.4 + 2.6 • Both 32 and 64 bit 	<ul style="list-style-type: none"> • Visual Basic, Visual C++, Borland C++ Builder, GNU C++, Borland Delphi, VB.NET • SBench, SPviewIT 	<ul style="list-style-type: none"> • MATLAB • LabVIEW, LabWindows • DASY Lab • Agilent VEE

Model	1-4 bit	8 bit	16 bit	32 bit	64 bit
M2i.7005	125 MS/s	125 MS/s	125 MS/s		
M2i.7010		125 MS/s	125 MS/s		
M2i.7011		125 MS/s	125 MS/s	60 MS/s	
M2i.7020		125 MS/s	125 MS/s	125 MS/s	
M2i.7021		125 MS/s	125 MS/s	125 MS/s	60 MS/s

General Information

The M2i.70xx series of fast digital I/O boards offer a resolution between 1 bit and 64 bit with a maximum sampling rate of 125 MS/s (60 MS/s). All I/O lines of the card can be programmed for either input or output direction. The on-board memory of up to 4 GByte can be used completely for recording or replaying digital data. Alternatively the M2i.70xx can be used in FIFO mode. All boards of the M2i.70xx series may use the whole installed on-board memory completely for the currently activated number of channels. Then data is transferred on-line to PC memory or hard disk. The internal standard synchronisation bus allows synchronisation of several M2i series cards. Therefore the M2i.70xx board can be used as an enlargement to analog boards.

*Some x16 PCIe slots are for the use of graphic cards only and can not be used for other cards.

Software Support

Windows drivers

The cards are delivered with drivers for Windows 2000, Windows XP, Windows XP64 and Windows Vista. Programming examples for Visual C/C++, Borland C++ Builder, LabWindows/CVI, Borland Delphi, Visual Basic and VB.NET are included.

Linux Drivers

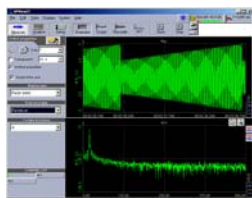


All cards are delivered with full Linux support. Pre compiled kernel modules are included for the most common distributions like RedHat, Fedora, Suse or Debian. The Linux support includes SMP systems, 32 bit and 64 bit systems, versatile programming examples for Gnu C++ as well as the possibility to get the driver sources for own compilation.

SBench

A full licence of SBench the easy-to-use graphical operating software for the Spectrum cards is included in the delivery. The version 6 is running under Windows as well as under Linux (KDE and GNOME).

SPViewIT



card.

SPviewIT is the professional streaming software solution for the Spectrum PC instruments. The software is optimised for continuous data acquisition of large amounts of data. Key features of SPviewIT are different data displays, editable interface and a huge amount of export filters. A demo version comes with the

Third-party products

A lot of third-party products are supported as an option. Choose between LabVIEW, MATLAB, DASYLab and Agilent VEE. All drivers come with examples and detailed documentation.

MI Software compatibility layer

To allow an easy change from MI cards to the new M2i cards for existing software a special software compatibility layer is delivered with the cards. This DLL converts MI calls to M2i calls and simulates a MI card in the software.

Hardware features and options

PCI/PCI-X



The M2i cards with PCI/PCI-X bus connector use 32 Bit and up to 66 MHz clock rate for data transfer. They are 100% compatible to Conventional PCI > V2.1. The universal interface allows the use in PCI slots with 5 V I/O and 3.3 V I/O voltages as well as in

PCI-X or PCI 64 slots. The maximum sustained data transfer rate is 225 MByte/s per bus segment.

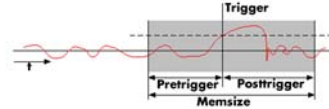
PCI Express



The M2i cards with PCI Express use a x1 PCIe connector. They can be used in PCI Express x1/x4/x8/x16 slots, except special graphic card slots, and are 100% software compatible to Conventional PCI > V2.1. The maxi-

imum sustained data transfer rate is 160 MByte/s per slot.

Ring buffer mode



The ring buffer mode is the standard mode of all oscilloscope boards. Data is written in a ring memory of the board until a trigger event is

detected. After the event the posttrigger values are recorded. Because of this continuously recording into a ring buffer there are also samples prior to the trigger event visible: Pretrigger = Memsize - Posttrigger.

FIFO mode

The FIFO mode is designed for continuous data transfer between measurement board and PC memory (up to 225 MB/s on a PCI-X slot and up to 115 MB/s on a PCI slot) or hard disk. The control of the data stream is done automatically by the driver on interrupt request. The complete installed on-board memory is used for buffer data, making the continuous streaming extremely reliable.

Pattern trigger

For every bit of the digital input the pattern trigger defines individually the expected level or sets the bit to „don't care“. In combination with pulsewidth counter and edge detection the pattern trigger could be used to recognise a huge variety of trigger events.

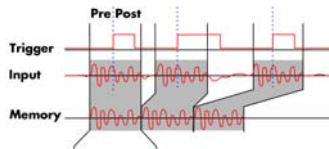
External trigger I/O

All digital boards can be triggered using an additional external TTL signal per acquisition module. It's possible to use positive or negative edge also in combination with a programmable pulse width. An internally recognized trigger event can - when activated by software - be routed to the trigger output connector to start external instruments.

Pulse width

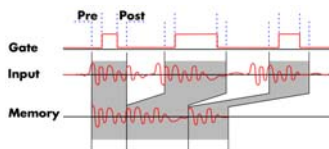
Defines the minimum or maximum width that a trigger pulse must have to generate a trigger event. Pulse width can be combined with channel trigger, pattern trigger and external trigger.

Multiple Recording



The Multiple Recording option allows the recording of several trigger events with an extremely short re-arming time. The hardware doesn't need to be restarted in between. The on-board memory is divided in several segments of the same size. Each of them is filled with data if a trigger event occurs. Pre- and posttrigger of the segments can be programmed. The number of acquired segments is only limited by the used memory and is unlimited when using FIFO mode.

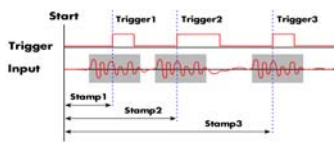
Gated Sampling



The Gated Sampling option allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a programmed level. In addition a pre-area before start

of the gate signal as well as a post area after end of the gate signal can be acquired. The number of gate segments is only limited by the used memory and is unlimited when using FIFO mode.

Timestamp



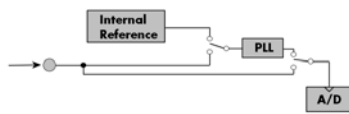
The timestamp option writes the time positions of the trigger events in an extra memory. The timestamps are relative to the start of recording, a defined zero time, externally synchronised to a radio clock, or a GPS receiver. With this option acquisitions of systems on different locations can be set in a precise time relation.

Externally synchronised to a radio clock, or a GPS receiver. With this option acquisitions of systems on different locations can be set in a precise time relation.

External clock I/O

Using a dedicated line a sampling clock can be fed in from an external system. It's also possible to output the internally used sampling clock to synchronize external equipment to this clock.

Reference clock



The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronise the board for high-quality

measurements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock in this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

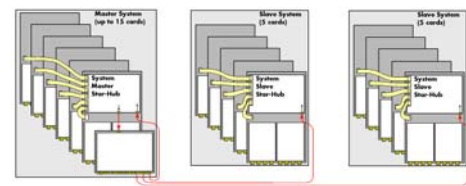
Star-Hub



The star-hub is an additional module allowing the phase stable synchronisation of up to 16 boards in one system. Independent of the number of boards there is no phase delay between all channels. The star-hub distributes trigger and

clock information between all boards. As a result all connected boards are running with the same clock and the same trigger. All trigger sources can be combined with OR/AND allowing all channels of all cards to be trigger source at the same time. The star-hub is available as 5 card and 16 card version. The 5 card version doesn't need an extra slot.

271 synchronous cards with the System Star-Hub



With the help of multiple system star-hubs it is possible to link up to 17 system phase synchronous with each other.

Each system can then contain up to 16 cards (master only 15). In total 271 cards can be used fully synchronously in a bunch of systems. One master system distributes clock and trigger signal to all connected slave systems.

1-4 bits mode

On the model 7005 it is also possible to use just 1, 2 or 4 bits for acquisition or replay. In 1 bit mode the 8 times higher memory is then available, at 2 bits mode it is 4 times higher and at 4 bits mode it is double. This enlarges the recording/replay time in on-board memory and it reduces the transfer rate when using FIFO mode. The data is stacked internally to 8 bit samples. Therefore all information on memory/segment/pre and posttrigger sizes and steps can be up to 8 times higher.

BaseXIO (enhanced trigger)



The BaseXIO option offers 8 asynchronous digital I/O lines on the base card. The direction can be selected by software in groups of four. Two of these lines can also be used as additional external trigger sources.

This allows the building of complex trigger conjunctions with external gated triggers as well as AND/OR conjunction of multiple external trigger sources like, for example, the picture and row synchronisation of video signals. In addition one of the I/O lines can be used as reference clock for the Timestamp counter.

Technical Data

Digital Inputs

Input Impedance (programmable)	110 Ohm / 50 kOhm 15 pF	
110 Ohm termination voltage	2.5V	
Standard input levels	Low ≤ 0.8 V, High ≥ 2.0 V	
Absolute maximum Input levels	≥ -0.5 V and ≤ 7.0 V	
Data Input current sink (no termination)	-1.0 μ A (0.0 V), +1.0 μ A (3.3V), +20.0 μ A (5.0V)	

Digital Outputs

Typical output levels (high impedance)	Low: 0.2 V	High: 2.8 V
Output max current load	Low: 64 mA	High: -32 mA
Output levels at max load	Low: < 0.5 V	High: > 2.0 V
Output Impedance (typical)	ca. 7 Ohms	

Output Delays

Trigger to 1st sample (≥ 8 active chan.)	19 clocks
Trigger to 1st sample (< 8 active chan.)	9 clocks + 10 * 8/active channels
Gate end to last replayed sample	19 samples (≥ 8 active channels)
Gate end alignment	[32 / active channels] in samples

Trigger

Available trigger modes	Pattern and mask, edge, external TTL, software, pulsewidth, Or/And, Delay
Pattern and mask	32 bit / 64 bit wide: 0 pattern, 1 pattern, don't care or edge
Trigger pulse width	0 to [64k - 1] samples in steps of 1 sample
Trigger delay	0 to [64k - 1] samples in steps of 1 sample
Multi/Gate re-arm time	< 4 samples (≥ 8 channels)
Max Pretrigger at Multi, Gate, FIFO	16352 bytes as sum of all active channels
Internal trigger accuracy	1 sample (≥ 8 active channels)
Trigger output delay	19 clocks
External trigger type	TTL compatible
External trigger input	Low ≤ 0.8 V, High ≥ 2.0 V, ≥ 2 clock periods
External trigger maximum voltage	-0.5 V up to +5.5 V
External trigger input current sink	± 1.0 μ A (no termination)
External trigger accuracy	1 sample (≥ 8 active channels)
External trigger accuracy	8/active channels samples (< 8 channels)
External trigger output levels	Low ≤ 0.4 V, High ≥ 2.4 V, TTL compatible
External trigger output drive strength	Capable of driving 110 and 50 ohm load
Trigger impedance (programmable)	110 Ohm / high impedance (> 4kOhm)

PCI / PCI-X specific details

PCI / PCI-X bus slot type	32 bit 33/66 MHz
PCI / PCI-X bus slot compatibility	32/64 bit, 33-133 MHz, 3,3 V and 5 V I/O

PCI EXPRESS specific details

PCIe slot type	x1
PCIe slot compatibility	x1/x4/x8/x16*

*Some x16 PCIe slots are for graphic cards only and can not be used for other cards.

Power consumption (max speed)

	PCI / PCI-X		PCI EXPRESS	
	3.3 V	5 V	3.3 V	12 V
M2i.7005/M2i.7010 (64 MB memory)	3.0 A	0.5 A	0.4 A	1.2 A
M2i.7011 (64 MB memory), 60 MS/s	3.2 A	0.5 A	0.4 A	1.1 A
M2i.7020 (64 MB memory), 125 MS/s	4.7 A	1.0 A	0.4 A	1.4 A
M2i.7021 (64 MB memory), 60 MS/s	5.4 A	0.9 A	0.4 A	1.3 A
M2i.7021 (4 GB memory), max. power	6.1 A	0.9 A	0.4 A	1.9 A

Max channels with Star-Hub Opt.

	SH5	SH16	SSH55	SSH516
M2i.7005, M2i.7010	80	256	1360	4336
M2i.7011, M2i.7020	160	512	2720	8672
M2i.7021 (each card needs 2 slots)	320	512	5440	8672

Clock

Available clock modes	PLL, Quartz, External, Reference Clock, External with Divider, Sync Clock
Internal clock range (PLL mode)	1 kS/s to max (see table below)
Internal clock accuracy	20 ppm
Internal clock: max. jitter in PLL mode	TBD
Internal clock: max. jitter in quartz mode	TBD
Internal clock setup granularity (≤ 100 M)	$\leq 1\%$ of range (100M, 10M, 1M, 100k,...)
Internal clock setup granularity example	range 1M to 10M: stepsize ≤ 100 k
Reference clock: external clock range	≥ 1.0 MHz and ≤ 125.0 MHz
External clock range	DC to max (see table below)
External clock input	Low ≤ 0.8 V, High ≥ 2.0 V, duty 45% - 55%
External clock delay to internal clock	15.8 ns (EXRANGE_LOW); 1.3 ns (others)
External clock maximum voltage	-0.5 V up to +5.5 V
External clock input current sink	± 1.0 μ A (no termination)
External clock output levels	Low ≤ 0.4 V, High ≥ 2.4 V, TTL compatible
External clock output drive strength	Capable of driving 110 and 50 ohm load
Clock Input impedance (programmable)	110 Ohm / high impedance (> 4kOhm)

Software programmable parameters

Data direction	Input/output for all channels
Memory depth	8 up to [installed memory / number of active channels] samples in steps of 4
Posttrigger	4 up to [8G - 4] samples in steps of 4
Multiple Recording segment size	8 up to [installed memory (Bytes) * 4 / active channels] samples in steps of 4
Multi / Gated pretrigger	0 up to [8 * 16k samples / number of active channels - 32]
ABA clock divider	1 up to [64k - 1] in steps of 1
Synchronization clock divider	2 up to [8k - 2] in steps of 2
Channel selection	1, 2, 4, 16, 32, or 64 digital channels (depending on card type)

BaseXIO (Option)

BaseXIO Connector (extra bracket)	8 x SMB (8 x MMCX internal)
BaseXIO input	TTL compatible: Low ≤ 0.8 V, High ≥ 2.0 V
BaseXIO input maximum voltage	-0.5 V up to +5.5 V
BaseXIO output levels	TTL compatible: Low ≤ 0.4 V, High ≥ 2.4 V
BaseXIO output drive strength	32 mA maximum current

Environmental and Physical details

Connector (digital inputs)	40 pole half pitch (Hirose FX2 series)
Dimension (PCB only)	312 mm x 107 mm (full PCI length)
Width (Standard or star-hub 5)	1 full size slot
Width (star-hub 16)	2 full size slots
Width (with BaseXIO)	1 full size slots + 1 half size slot
Weight (depending on type/options)	290g (16 ch) to 480g (64 ch all options)
Warm up time	instant on
Operating temperature	0°C - 50°C
Storage temperature	-10°C - 70°C
Humidity	10% to 90%

Power up

Data channels direction after power up	input (high impedance)
Clock and trigger output after power up	disabled

Certifications and Compliances

EMC Immunity	Compliant with CE Mark
EMC Emission	Compliant with CE Mark

External clock-to-data timing

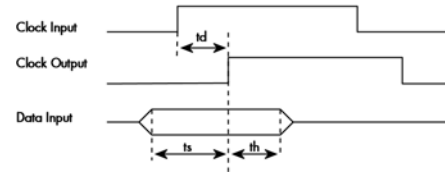
The setup and hold times as well as any delays relate to the output clock. If using external clock the timing depends on the used external range. Please be sure to meet this timing constraints if feeding in external clock.

For detailed information on the different modes for external clocking please refer to the dedicated chapter in the hardware manual for the boards of the M2i.70xx series.

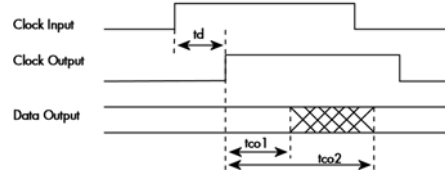
Delay time	External Clocking Mode			Internal Clocking
	EXRANGE_LOW	EXRANGE_LOW_DPS	EXRANGE_HIGH	
t_d	16.9 ns	1.6 ns	1.6 ns	n.a.
t_{co1}	2.0 ns	2.0 ns	2.0 ns	2.0 ns
t_{co2}	5.8 ns	5.8 ns	5.8 ns	5.8 ns
t_s	2.1 ns	2.1 ns	2.1 ns	2.1 ns
t_h	0.7 ns	0.7 ns	0.7 ns	0.7 ns

When using external clock a delayed clock signal is generated on the Clock Output pin. The timing data in relation to this delayed clock output is similar to the timing when using internal clocking. It is therefore strongly recommended that you use the delay clock output for clocking any external devices.

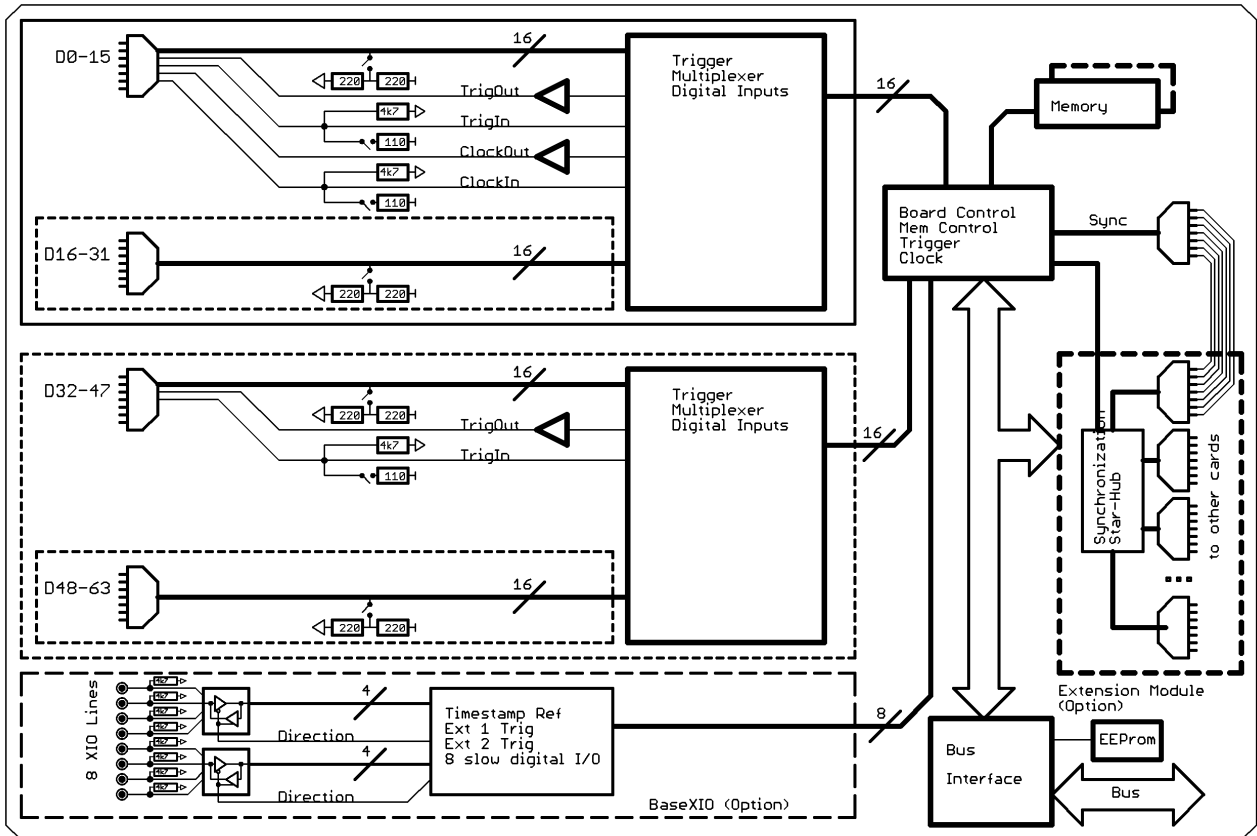
Input timing



Output timing



Hardware block diagram



Order Information

PCI/PCI-X

Order no.	Std Mem	1 Bit	2 Bit	4 Bit	8 Bit	16 Bit	32 Bit	64 Bit
M2i.7005	64 MB	125 MS/s	125 MS/s	125 MS/s	125 MS/s	125 MS/s		
M2i.7010	64 MB	-	-	-	125 MS/s	125 MS/s		
M2i.7011	64 MB	-	-	-	125 MS/s	125 MS/s	60 MS/s	
M2i.7020	64 MB	-	-	-	125 MS/s	125 MS/s	125 MS/s	
M2i.7021	64 MB	-	-	-	125 MS/s	125 MS/s	125 MS/s	60 MS/s

PCI Express

Order no.	Std Mem	1 Bit	2 Bit	4 Bit	8 Bit	16 Bit	32 Bit	64 Bit
M2i.7005-exp	64 MB	125 MS/s	125 MS/s	125 MS/s	125 MS/s	125 MS/s		
M2i.7010-exp	64 MB	-	-	-	125 MS/s	125 MS/s		
M2i.7011-exp	64 MB	-	-	-	125 MS/s	125 MS/s	60 MS/s	
M2i.7020-exp	64 MB	-	-	-	125 MS/s	125 MS/s	125 MS/s	
M2i.7021-exp	64 MB	-	-	-	125 MS/s	125 MS/s	125 MS/s	60 MS/s

Memory

Order no.	Option
M2i.xxxx-128MB	Memory upgrade to 128 MB of total memory
M2i.xxxx-256MB	Memory upgrade to 256 MB of total memory
M2i.xxxx-512MB	Memory upgrade to 512 MB of total memory
M2i.xxxx-1GB	Memory upgrade to 1 GB of total memory
M2i.xxxx-2GB	Memory upgrade to 2 GB of total memory
M2i.xxxx-4GB	Memory upgrade to 4 GB of total memory

Options

Order no.	Option
M2i.xxxx-mr	Option Multiple Recording/Replay
M2i.xxxx-mgt	Option pack including Multiple Recording/Replay, Gated Sampling/Replay, Timestamp
M2i.xxxx-SH5 (1)	Synchronization Star-Hub for up to 5 cards, only 1 slot width
M2i.xxxx-SH16 (1)	Synchronization Star-Hub for up to 16 cards
M2i.xxxx-SSHM (1)	System-Star-Hub Master for up to 15 cards in the system and up to 17 systems, sync cables included
M2i.xxxx-SSHS5 (1)	System-Star-Hub Slave for up to 5 cards in one system, all sync cables included
M2i.xxxx-SSHS16 (1)	System-Star-Hub Slave for up to 16 cards in one system, all sync cables included
M2i.xxxx-bxio	Option BaseXIO: 8 digital I/O lines usable as asynchronous I/O, timestamp ref-clock and additional external trigger lines, additional bracket with 8 SMB connectors
M2i-upgrade	Upgrade for M2i.xxxx: later installation of option -dig or -bxio

Cables

Order no.	Option
Cab-3f-9m-80	Adapter cable SMB female to BNC male, 80 cm
Cab-3f-9f-80	Adapter cable SMB female to BNC female, 80 cm
Cab-3f-3f-80	Adapter cable SMB female to SMB female, 80 cm
Cab-3f-9m-200	Adapter cable SMB female to BNC male, 200 cm
Cab-3f-9f-200	Adapter cable SMB female to BNC female, 200 cm
Cab-3f-3f-200	Adapter cable SMB female to SMB female, 200 cm
Cab-3f-9f-5	Adapter cable SMB female to BNC female, 5 cm (short cable especially for oscilloscopes probes)
Cab-d40-idc-100	Flat ribbon cable 40 pole FX2 for digital connector to 2x20 pole IDC connector, 100 cm
Cab-d40-d40-100	Flat ribbon cable 40 pole FX2 for digital connector to 40 pole digital FX2 connector, 100 cm

Drivers

Order no.	Option
M2i.xxxx-ml	MATLAB driver for all M2i cards
M2i.70xx-lv	LabVIEW driver for all M2i.70xx cards
M2i.70xx-dl	DASLab driver for all M2i.70xx cards
M2i.70xx-vee	Agilent VEE driver for all M2i.70xx cards

(1) : Just one of the options can be installed on a card at a time.

technical changes and printing errors possible