

Krenz *Instrumentation*

M2i.72xx - 32 bit pattern generator with programmable levels

- Programmable output levels from -2,0 V up to +10,0 V
- Levels individually programmable per 4 bit
- Up to 40 MS/s at 32 bit
- All Outputs can be separately disabled (Tristate)
- Hardware controlled differential output possible
- Up to 4 GByte on-board memory
- 64 MByte standard memory installed
- FIFO mode for input and output
- Sustained streaming mode
- Pattern/edge/pulse width/delay trigger
- Synchronization of up to 16 cards per system and up to 271 cards with system sync
- Options: Multiple Replay, Gated Replay, BaseXIO



- 66 MHz 32 Bit PCI-X interface
- 5V / 3.3V PCI compatible
- 100% compatible to conventional PCI > V2.1
- Sustained streaming mode up to 225 MB/s

- 2,5 GBit x1 PCIe Interface
- Works with x1/x4/x8/x16* PCIe slots
- Software compatible to PCI
- Sustained streaming mode up to 160 MB/s

<u>Operating Systems</u>	<u>Recommended Software</u>	<u>Drivers</u>
<ul style="list-style-type: none"> • Windows 2k, XP, Vista • Linux Kernel 2.4 + 2.6 • Both 32 and 64 bit 	<ul style="list-style-type: none"> • Visual Basic, Visual C++, Borland C++ Builder, GNU C++, Borland Delphi, VB.NET • SBench, SPviewIT 	<ul style="list-style-type: none"> • MATLAB • LabVIEW, LabWindows • DASY Lab • Agilent VEE

Model	1-4 bit	8 bit	16 bit	32 bit
M2i.7210	10 MS/s	10 MS/s	10 MS/s	
M2i.7211	10 MS/s	10 MS/s	10 MS/s	5 MS/s
M2i.7220	40 MS/s	40 MS/s	40 MS/s	
M2i.7221	40 MS/s	40 MS/s	40 MS/s	40 MS/s

General Information

The M2i.72xx pattern generator series gives the user the possibility to generate digital data with a wide range of output levels. For every 4 bit the LOW and HIGH levels can be programmed from -2.0 V up to +10.0 V. Even at high speeds you are not limited concerning the maximum output swing. This enables the user to drive devices of nearly any logic family, like ECL, PECL, TTL, LVDS, LVTTTL, CMOS or LVCMOS. The potentially necessary differential signals are generated in hardware, so that only one data bit is used for each pair of differential signals. The on-board memory of up to 4 GByte can be used completely for recording or replaying digital data. Alternatively the M2i.70xx can be used in FIFO mode. Then data is transferred on-line from PC memory or hard disk. All boards of the M2i.72xx series may use the whole installed on-board memory completely for the currently activated number of channels.

*Some x16 PCIe slots are for the use of graphic cards only and can not be used for other cards.

Software Support

Windows drivers

The cards are delivered with drivers for Windows 2000, Windows XP, Windows XP64 and Windows Vista. Programming examples for Visual C/C++, Borland C++ Builder, LabWindows/CVI, Borland Delphi, Visual Basic and VB.NET are included.

Linux Drivers



All cards are delivered with full Linux support. Pre compiled kernel modules are included for the most common distributions like RedHat, Fedora, Suse or Debian. The Linux support includes SMP systems, 32 bit and 64 bit systems, versatile programming examples for Gnu C++ as well as the possibility to get the driver sources for own compilation.

SBench

A full licence of SBench the easy-to-use graphical operating software for the Spectrum cards is included in the delivery. The version 6 is running under Windows as well as under Linux (KDE and GNOME).

Third-party products

A lot of third-party products are supported as an option. Choose between LabVIEW, MATLAB, DASYLab and Agilent VEE. All drivers come with examples and detailed documentation.

MI Software compatibility layer

To allow an easy change from MI cards to the new M2i cards for existing software a special software compatibility layer is delivered with the cards. This DLL converts MI calls to M2i calls and simulates a MI card in the software.

Hardware features and options

PCI/PCI-X



The M2i cards with PCI/PCI-X bus connector use 32 Bit and up to 66 MHz clock rate for data transfer. They are 100% compatible to Conventional PCI > V2.1. The universal interface allows the use in PCI slots with 5 V I/O and 3.3 V I/O voltages as well as in

PCI-X or PCI 64 slots. The maximum sustained data transfer rate is 225 MByte/s per bus segment.

PCI Express



The M2i cards with PCI Express use a x1 PCIe connector. They can be used in PCI Express x1/x4/x8/x16 slots, except special graphic card slots, and are 100% software compatible to Conventional PCI > V2.1. The maximum sustained data transfer rate is

160 MByte/s per slot.

FIFO mode

The FIFO mode is designed for continuous data transfer between measurement board and PC memory (up to 225 MB/s on a PCI-X slot and up to 115 MB/s on a PCI slot) or hard disk. The control of the data stream is done automatically by the driver on interrupt request. The complete installed on-board memory is used for buffer data, making the continuous streaming extremely reliable.

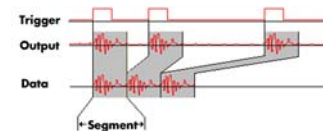
External trigger I/O

All digital boards can be triggered using an additional external TTL signal per acquisition module. It's possible to use positive or negative edge also in combination with a programmable pulse width. An internally recognized trigger event can - when activated by software - be routed to the trigger output connector to start external instruments.

Pulse width

Defines the minimum or maximum width that a trigger pulse must have to generate a trigger event. Pulse width can be combined with channel trigger, pattern trigger and external trigger.

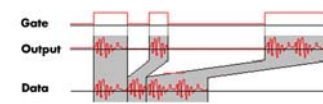
Multiple Replay



The Multiple Replay option allows the fast repetition output on several trigger events without restarting the hardware. With this option very fast repetition rates can be achieved.

The on-board memory is divided in several segments of same size. Each of them is generated if a trigger event occurs.

Gated Replay



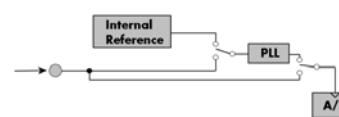
The Gated Sampling option allows data replay controlled by an external gate signal. Data is only replayed if the gate signal has a pro-

grammed level.

External clock I/O

Using a dedicated line a sampling clock can be fed in from an external system. It's also possible to output the internally used sampling clock to synchronize external equipment to this clock.

Reference clock



The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronise the board for high-quality

measurements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock in this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

Singleshot output

When singleshot output is activated the data of the on-board memory is replayed exactly one time. As trigger source one can use the external TTL trigger or the software trigger.

Repeated output

When repeated output is used the data of the on-board memory is replayed continuously until a stop command is executed or N times. As trigger source one can use the external TTL trigger or the software trigger.

Single Restart replay

When this mode is activated the data of the on-board memory will be replayed once after each trigger event. Trigger source one can use the external TTL or software trigger.

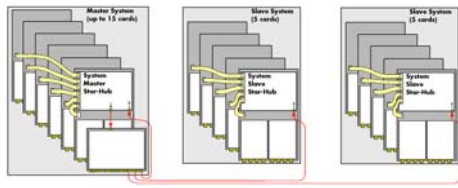
Star-Hub



The star-hub is an additional module allowing the phase stable synchronisation of up to 16 boards in one system. Independent of the number of boards there is no phase delay between all channels. The star-hub distributes trigger and

clock information between all boards. As a result all connected boards are running with the same clock and the same trigger. All trigger sources can be combined with OR/AND allowing all channels of all cards to be trigger source at the same time. The star-hub is available as 5 card and 16 card version. The 5 card version doesn't need an extra slot.

271 synchronous cards with the System Star-Hub



With the help of multiple system star-hubs it is possible to link up to 17 system phase synchronous with each other.

Each system can then contain up to 16 cards (master only 15). In total 271 cards can be used fully synchronously in a bunch of systems. One master system distributes clock and trigger signal to all connected slave systems.

1-4 bits mode

On all models it is also possible to use just 1, 2 or 4 bits for replay. In 1 bit mode the 8 times higher memory is then available, at 2 bits mode it is 4 times higher and at 4 bits mode it is double. This enlarges the replay time in on-board memory and it reduces the transfer rate when using FIFO mode. The data is stacked internally to 8 bit samples. Therefore all information on memory/segment/pre and posttrigger sizes and steps can be up to 8 times higher.

BaseXIO (enhanced trigger)



The BaseXIO option offers 8 asynchronous digital I/O lines on the base card. The direction can be selected by software in groups of four. Two of these lines can also be used as additional external trigger sources. This allows the building of complex trigger conjunctions with external gated triggers as well as AND/OR conjunction of multiple external trigger sources like, for example, the picture and row synchronisation of video signals. In addition one of the I/O lines can be used as reference clock for the Timestamp counter.

Technical Data

Outputs

Output impedance	approximately 80 Ohm
Data signal level	programmable from -2.0 V up to +10.0 V
Programmable level accuracy	±10 mV
Max output current per pin	100 mA
Max output current per nibble (4 bit)	200 mA
Max output current per	500 mA (M2i.721x cards, otherwise no limit)
Rise/Fall time 10% to 90%, 110 ohm	2.0 ns (1 MS/s) up to 2.25 ns (40 MS/s)
Connector	40 pole half pitch (Hirose FX2 series)

Trigger

Multi, Gate: re-arming time	<4 samples (≥ 8 active channels)
Max Pretrigger at Multi, Gate, FIFO	16352 bytes as sum of all active channels
Internal trigger accuracy	1 sample (≥ 8 active channels)
External trigger type	TTL compatible
External trigger input	Low ≤ 0.8 V, High ≥ 2.0 V, ≥ 2 clock periods
External trigger maximum voltage	-0.5 V up to +5.5 V
External trigger input current sink	± 1.0 µA (no termination)
External trigger accuracy	1 sample (≥ 8 active channels)
External trigger accuracy	8/active channels samples (< 8 channels)
External trigger output levels	Low ≤ 0.4 V, High ≥ 2.4 V, TTL compatible
External trigger output drive strength	Capable of driving 110 and 50 ohm load

Environmental and Physical details

Dimension (PCB only)	312 mm x 107 mm (full PCI length)
Width (standard or sh5) M2i.721x	1 full size slot
Width (star-hub 16) or M2i.722x	2 full size slots
Width (with BaseXIO) M2i.721x	1 full size slots + 1 half size slot
Width (with BaseXIO) M2i.722x	2 full size slots + 1 half size slot
Weight (depends on options/channels)	290g (7210) to 570g (7221 all options)
Warm up time	instant on
Operating temperature	0°C - 50°C
Storage temperature	-10°C - 70°C
Humidity	10% to 90%

Power up

Data channels state after power up	tristate (high impedance)
Clock and trigger output after power up	disabled

Power consumption (max speed) (Power Source)	3.3 V	5 V	+12 V	+12 V
	Bus	Bus	Bus	Cable
M2i.7210 (64 MB memory)	TBD	TBD	0.35 A	-
M2i.7211 (64 MB memory)	TBD	TBD	0.40 A	-
M2i.7220 (64 MB memory)	TBD	TBD	-	1.8 A
M2i.7221 (64 MB memory)	TBD	TBD	-	3.6 A
M2i.7221 (4 GB memory), max. power	TBD	TBD	-	3.6 A
M2i.7210-Exp (64 MB memory)	0.4 A	n.a.	TBD	-
M2i.7211-Exp (64 MB memory)	0.4 A	n.a.	TBD	-
M2i.7220-Exp (64 MB memory)	0.4 A	n.a.	TBD	TBD
M2i.7221-Exp (64 MB memory)	0.4 A	n.a.	TBD	TBD
M2i.7221-Exp (4 GB memory)	0.4 A	n.a.	TBD	TBD

Max channels with Star-Hub Opt.

	SH5	SH16	SSH55	SSH516
M2i.7220 (each card needs 2 slots)	40	128	680	2218
M2i.7210, M2i.7221 (needs 2 slots)	80	256	1360	4336
M2i.7211	160	512	2720	8672

Clock

Internal clock modes	PLL, Quartz, Custom Quartz
External clock modes	Direct, Ext. divided, Reference clock
Internal clock range (PLL mode)	1 kS/s to max (see table below)
Internal clock accuracy	20 ppm
Internal clock: max. jitter in PLL mode	TBD
Internal clock: max. jitter in quartz mode	TBD
Internal clock setup granularity (≤ 100 M)	≤1% of range (100M, 10M, 1M, 100k,...)
Internal clock setup granularity example	range 1M to 10M: stepsize ≤ 100k
Reference clock: external clock range	≥ 1.0 MHz and ≤ 125.0 MHz
External clock range	DC to max (see table below)
External clock delay to internal clock	14.9 ns (EXRANGE_LOW); 1.3 ns (others)
External clock input	Low ≤ 0.8 V, High ≥ 2.0 V, duty 45% - 55%
External clock maximum voltage	-0.5 V up to +5.5 V
External clock input current sink	± 1.0 µA (no termination)
External clock output levels	Low ≤ 0.4 V, High ≥ 2.4 V, TTL compatible
External clock output drive strength	Capable of driving 110 and 50 ohm load

BaseXIO (Option)

BaseXIO Connector (extra bracket)	8 x SMB (8 x MMCX internal)
BaseXIO input	TTL compatible: Low ≤ 0.8 V, High ≥ 2.0 V
BaseXIO input maximum voltage	-0.5 V up to +5.5 V
BaseXIO output levels	TTL compatible: Low ≤ 0.4 V, High ≥ 2.4 V
BaseXIO output drive strength	32 mA maximum current

Output Delays

Trigger to 1st sample (≥ 8 active chan.)	18 clocks
Trigger to 1st sample (< 8 active chan.)	8 clocks + 10 * 8/active channels
Gate end to last replayed sample	18 samples (≥ 8 active channels)
Gate end alignment	[32 / active channels] in samples

Software programmable parameters

Clock impedance	110 Ohm / high impedance (> 4kOhm)
Trigger impedance	110 Ohm / high impedance (> 4kOhm)
Trigger mode	External TTL, software, pulsewidth, Delay
Trigger pulse width	0 to [64k - 1] samples in steps of 1 sample
Trigger edge	Rising edge, falling edge, both edges
Trigger delay	0 to [64k - 1] samples in steps of 1 sample
Memory depth	8 up to [inst mem / channels] in steps of 4
Posttrigger	4 up to [8G - 4] samples in steps of 4
Multiple Recording segment size	8 up to [inst mem / channels] in steps of 4
Synchronization clock divider	2 up to [8k - 2] in steps of 2
Channel selection	1, 2, 4, 16 or 32 digital channels

PCI / PCI-X specific details

PCI / PCI-X bus slot type	32 bit 33/66 MHz
PCI / PCI-X bus slot compatibility	32/64 bit, 33-133 MHz, 3.3V and 5V I/O

PCI EXPRESS specific details

PCIe slot type	x1
PCIe slot compatibility	x1/x4/x8/x16*

*Some x16 PCIe slots are for graphic cards only and can not be used for other cards.

Certifications and Compliances

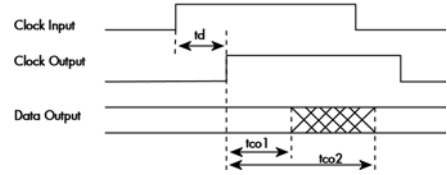
EMC Immunity	Compliant with CE Mark
EMC Emission	Compliant with CE Mark

External clock-to-data timing

The setup and hold times as well as any delays relate to the output clock. If using external clock the timing depends on the used external range. Please be sure to meet this timing constraints if feeding in external clock.

For detailed information on the different modes for external clocking please refer to the dedicated chapter in the hardware manual for the boards of the M2i.72xx series.

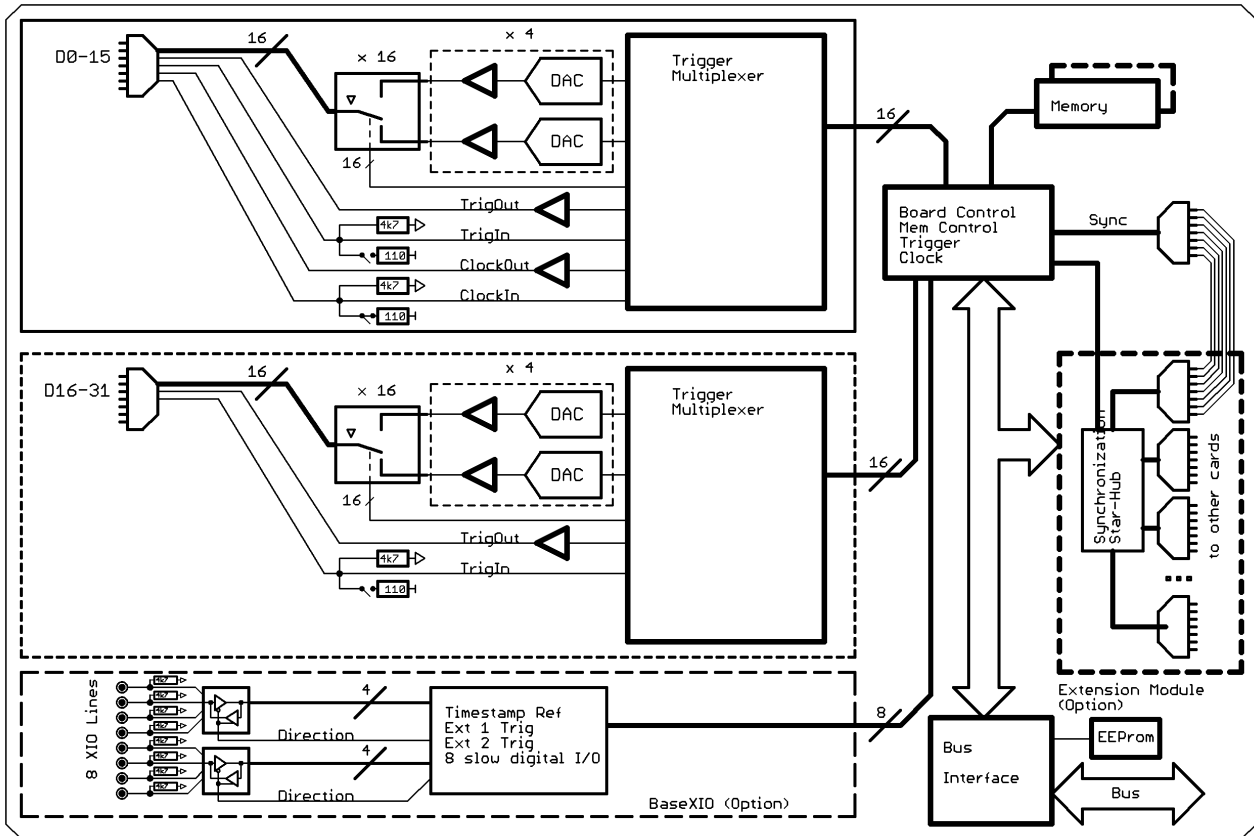
Output timing



Delay time	External Clcking Mode		Internal Clcking
	EXRANGE_LOW	EXRANGE_LOW_DPS	
t_d	17.9 ns	4.3 ns	n.a.
t_{co1}	TBD	TBD	TBD
t_{co2}	TBD	TBD	TBD

When using external clock a delayed clock signal is generated on the Clock Output pin. The timing data in relation to this delayed clock output is similar to the timing when using internal clocking. It is therefore strongly recommended that you use the delay clock output for clocking any external devices.

Hardware block diagram



Order Information

PCI/PCI-X

Order no.	Standard Mem	1 Bit	2 Bit	4 Bit	8 Bit	16 Bit	32 Bit
M2i.7210	64 MB	10 MS/s	10 MS/s	10 MS/s	10 MS/s	10 MS/s	
M2i.7211	64 MB	10 MS/s	10 MS/s	10 MS/s	10 MS/s	10 MS/s	5 MS/s
M2i.7220	64 MB	40 MS/s	40 MS/s	40 MS/s	40 MS/s	40 MS/s	
M2i.7221	64 MB	40 MS/s	40 MS/s	40 MS/s	40 MS/s	40 MS/s	40 MS/s

PCI Express

Order no.	Standard Mem	1 Bit	2 Bit	4 Bit	8 Bit	16 Bit	32 Bit
M2i.7210-exp	64 MB	10 MS/s	10 MS/s	10 MS/s	10 MS/s	10 MS/s	
M2i.7211-exp	64 MB	10 MS/s	10 MS/s	10 MS/s	10 MS/s	10 MS/s	5 MS/s
M2i.7220-exp	64 MB	40 MS/s	40 MS/s	40 MS/s	40 MS/s	40 MS/s	
M2i.7221-exp	64 MB	40 MS/s	40 MS/s	40 MS/s	40 MS/s	40 MS/s	40 MS/s

Memory

Order no.	Option
M2i.xxxx-128MB	Memory upgrade to 128 MB of total memory
M2i.xxxx-256MB	Memory upgrade to 256 MB of total memory
M2i.xxxx-512MB	Memory upgrade to 512 MB of total memory
M2i.xxxx-1GB	Memory upgrade to 1 GB of total memory
M2i.xxxx-2GB	Memory upgrade to 2 GB of total memory
M2i.xxxx-4GB	Memory upgrade to 4 GB of total memory

Options

Order no.	Option
M2i.xxxx-mr	Option Multiple Replay
M2i.xxxx-gs	Option Gated Replay
M2i.xxxx-SH5 (1)	Synchronization Star-Hub for up to 5 cards, only 1 slot width
M2i.xxxx-SH16 (1)	Synchronization Star-Hub for up to 16 cards
M2i.xxxx-SSHM (1)	System-Star-Hub Master for up to 15 cards in the system and up to 17 systems, sync cables included
M2i.xxxx-SSHS5 (1)	System-Star-Hub Slave for up to 5 cards in one system, all sync cables included
M2i.xxxx-SSHS16 (1)	System-Star-Hub Slave for up to 16 cards in one system, all sync cables included
M2i.xxxx-bxio	Option BaseXIO: 8 digital I/O lines usable as asynchronous I/O and additional external trigger lines, additional bracket with 8 SMB connectors
M2i-upgrade	Upgrade for M2i.xxxx: later installation of option -dig or -bxio

Cable

Order no.	Option
Cab-d40-idc-100	Flat ribbon cable 40 pole FX2 for digital connector to 2x20 pole IDC connector, 100 cm
Cab-d40-d40-100	Flat ribbon cable 40 pole FX2 for digital connector to 40 pole digital FX2 connector, 100 cm

Drivers

Order no.	Option
M2i.xxxx-ml	MATLAB driver for all M2i cards
M2i.70xx-lv	LabVIEW driver for all M2i.70xx cards
M2i.70xx-dl	DASyLab driver for all M2i.70xx cards
M2i.70xx-vee	Agilent VEE driver for all M2i.70xx cards

(1) : Just one of the options can be installed on a card at a time.

technical changes and printing errors possible